Update plan of the existing beam interlock system for the RIBF†

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We report on the update plan of the existing beam interlock system (BIS). The BIS is a system that protects the hardware of RIBF accelerators from potential damage caused by accidental irradiation of high-power heavy-ion beams.[1] It was designed to stop beams within 10 ms after receiving an alarm signal from the accelerator and beam transport line components. On receiving an alarm signal, the BIS outputs a signal to one of the beam choppers installed just below the ion source, which deflects the beam immediately. The BIS was developed based on the Melsec-Q series programmable logic controllers (PLCs). The hardware configuration of the BIS is shown in the left part of Fig. 1.

The existing BIS began its operation in 2006, along with the beam commissioning of RIBF. In addition to an increase in the number of input signals to the BIS over 10 years of operation, too much information is shared among all the stations through optical links in the BIS. The response time becomes 15–20 ms, which is greater than its design value. On the other hand, the beam power has exceeded 10 kW recently, and beam operation at the level of several tens of kW is expected in the near future.[2] To handle higher-power beams more safely, a response speed of 10 ms or less is required for the BIS, in order to suppress the hardware damage caused by high-power beams. In addition, a greater number of components than those included in the present BIS have to be carefully monitored because subtler failures can potentially cause severe accidents in the case of very high-power beams. However, there is a limit for the existing BIS to reduce the response speed for the increasing number of associated components. Therefore, we have commenced the development of the next-generation BIS (hereinafter, BIS2), which is designed to have advanced performance and convenience in operation compared to the existing BIS.

The BIS2 implements interlock logic, which is fundamentally equivalent to that of the existing BIS. Based on the operation experience of more than 10 years of the existing BIS, we decided to develop the BIS2 system by ourselves from scratch. Furthermore, we designed it to reduce the amount of data shared between different stations in the BIS2 in order to reduce the response time. In the BIS2, only the output signal status is shared among stations. As a device satisfying the above requirements, we adopted the FA-M3 PLC system. As a prototype of the BIS2, we adopt the two-station configuration; however, there is no technical limit to the number of stations and the number of I/O points included in the BIS2.

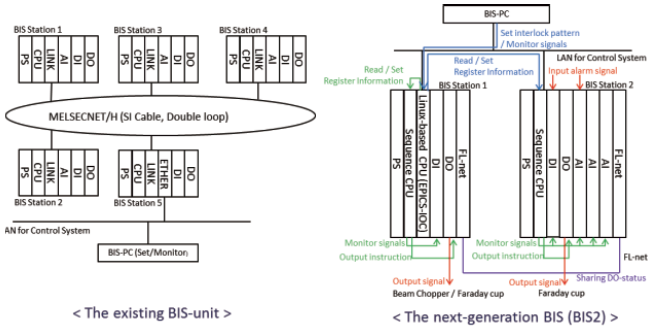

Fig. 1. Hardware configuration of the existing BIS (left) and the BIS2 (right).

The right part of Fig. 1 shows the hardware constitution and the process flow of the BIS2 prototype. The system employs a multi-CPU configuration; the sequence CPU, the Linux-based CPU (hereinafter, F3RP61 CPU), I/O modules, and FL-net module are mounted on one station, and the sequence CPU, I/O modules, and FL-net module are mounted on the other station. We plan to have coupled operation of the BIS2 to the main RIBF control system based on EPICS. Interlock logic is implemented in the sequence CPU, because high-speed processing and high reliability are required. Such high-speed processing is not necessary for setting and monitoring the interlock signal; these functions are implemented in the F3RP61 CPU. We execute EPICS on the F3RP61 CPU and access it from the upper-level PC via Ethernet. The interlock signal information transfer between two stations is performed through FL-net: an open network protocol used for interconnection between controllers.

We plan to apply the BIS2 prototype to the AVF cyclotron and its low-energy experimental facility, as a first step in the RIBF BIS upgrade. By simulating the AVF cyclotron facility, we conducted basic performance tests. First, we verified that the BIS2 prototype outputs signals correctly when the pattern of input signals is changed. Next, we measured the signal transmission speed in the system using an oscilloscope. As a result, the average response time in the same station was found to be 1.4 ms, and when the signal input and output were carried out at different stations, the average response time was 3.8 ms. The measured response speed is better than the specification required in the BIS2 development. Online operation of the BIS2 prototype at the AVF site is scheduled in 2018.

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