# Start the operation of AVF-BIS and its performance evaluation as a successor system to BIS

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The beam interlock system (BIS) for machine protection began operation in 2006 along with the beam commissioning of RIBF.[1)] The BIS is still under stable operation; however, its maintenance has become gradually difficult because some of the modules used in the system are discontinued and cannot be replaced. In addition, another problem is the declining performance of the system because of the increase in the number of inputs to the system during its 14 years of operation. Measurements performed in summer 2020 show that the average response time of BIS, the time from when the system receives the interlock signal to when the beam is stopped, is approximately 18 ms, which is greater than the system design value of 10 ms. To operate higher-power beams in the future more safely, a response speed of 10 ms or less is required. Therefore, we have been developing a successor system to the BIS for a few years, and we applied the prototype to the AVF cyclotron and its low-energy experimental facility as AVF-BIS in summer 2020. We will report its operation status and performance evaluation.

The hardware constitution and process flow of the prototype are shown in Fig. 1; the details are reported in Ref. 2). One new advantage of the prototype is that it has a multi-central processing unit (CPU) configuration that can shorten the response time of the system by using different CPUs according to the speed required by each process such as stopping the beam after receiving the interlock signal and parameter setting of the system. We set up the prototype comprising two programmable logic controller (PLC) stations: one with a Linux-based CPU and a sequence CPU was installed in the vault for the polarized ion source, and the other with a sequence CPU was installed in vault C for the power supplies for the magnets. The communication between the two stations was performed through FL-net (an open network protocol used for interconnection between controllers) using dedicated wiring; the signal setting and monitoring are performed by the terminal in the control room via the Ethernet. In AVF-BIS, 25 digital inputs and 24 analog inputs are used as the interlock signals; 5 digital outputs are used to stop a beam in total.

As a result of the oscilloscope-measured signal transmission speed in the AVF-BIS, the observed response time averaged 2 ms and 5.7 ms, respectively, within one station and with both stations. The average response time is 1.4 ms and 3.8 ms for the operation within one station and using two stations, respectively, in the test prior to the introduction of the prototype as AVF-BIS. The difference between the two measurements is attributed to the difference in the length of the ladder program executed on the sequence CPU: the ladder program became longer as a result of the repeated program modifications when operating the prototype as the AVF-BIS. However, it is sufficient as the performance of the AVF-BIS. When deploying the AVF-BIS in the same scale as the BIS that consists of 5 PLC stations with roughly 400 signals, the response time is estimated to be almost 10 ms. The basis for the estimation is as follows: increase the number of total signals and the time required for the signal transmission via FL-net increases depending on the number of PLC stations.

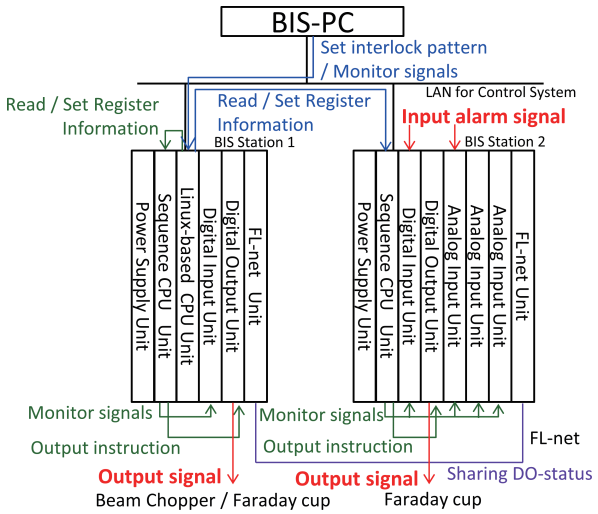


Fig. 1. Hardware constitution and process flow in the prototype. Blue lines represent communication via Ethernet, green lines represent communication via PLC bus, and purple lines represent communication via FL-net.

The above result shows that it is possible to achieve half the response time of the existing BIS by expanding the prototype to the successor system of the BIS; however, simultaneously, it shows that it limits the performance of the system. In a system with insufficient performance, it may not be possible to maintain the increase in the number of signals required to be monitored by the BIS in the future when a higher-power beam accelerated by RIBF, and another higher performance system may be required again. To avoid such a scenario, we have started to study a system with a field-programmable gate array (FPGA). The process that requires high speed is executed on the FPGA while the system is designed based on PLC. The system aims to reduce the response time to digital input signals to less than 1 ms.

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References

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