Development of FPGA-based machine protection system for RIBF

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We have been investigating a new machine protection system that will succeed the existing beam interlock system (BIS)[1] of RIBF since the latter half of 2020. The hardware configuration and the process flow in the BIS are shown in Fig. 1, where programmable logic controllers (PLCs) are used to process interlock signals. The typical response time of BIS is 18 ms, which will be insufficient for higher-intensity beams expected in the near future. Therefore, we plan to introduce a field-programmable gate array (FPGA) to process interlock signals, aiming at reducing the response time for digital input signals to less than 1 ms.

In the development of a BIS system using FPGAs (hereinafter, FPGA-BIS), the method of stopping a beam to protect the machine is basically the same as that of the BIS and AVF-BIS.[2] Each station that composes the FPGA-BIS will be installed at or near the existing BIS station to maximally reuse the existing signal wirings of the BIS. Therefore, the stations are widely distributed in the facility as well as in the BIS.

Based on the experience of operating BIS and AVF-BIS, we plan to use FPGAs and central processing units (CPUs) properly according to the signal processing time required. Various interlock conditions are imposed on the existing BIS and FPGA-BIS for each input signal. In essence, the process from the input of an alarm signal to the stopping of the beam through the evaluation of interlock conditions is performed on the FPGA, and the condition setting for and monitoring of each signal are performed from a host server via the CPU. As in the case of the AVF-BIS, the EPICS will be executed on the CPU.

In addition, since the BIS outputs a signal to the beam choppers, the FPGA-BIS implements not only the function of BIS, but also a function of controlling the beam intensity by using a beam chopper. Consequently, it can be expected that the system for sending signals to the beam choppers will be simplified relative to the current situation.

To achieve the performance required in FPGA-BIS, we compared two candidates: FA-M3 series PLC with the addition of input/output (I/O) modules with an FPGA (FPIO module, F3DF01-0N)[3] and CompactRIO, a product by National Instruments.[4] We concluded that both systems can meet the required performance as FPGA-BIS. Construction costs were also evaluated for both the systems with the same scale as the existing BIS, and we found that the construction cost using CompactRIO is about half of that using the FA-M3 PLCs. In a logic development of FPGA on the CompactRIO system, LabVIEW,[5] which has many useful functions and makes programming easier, can be used.

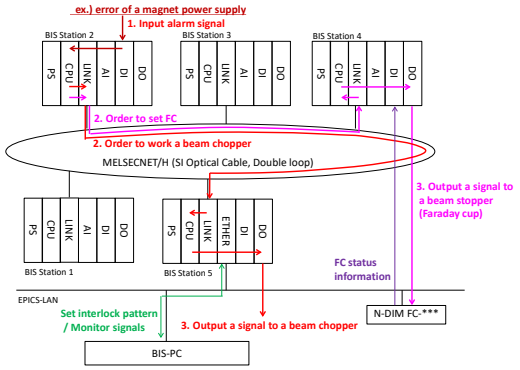

Fig. 1. Hardware configuration and process flow in BIS.

Therefore, CompactRIO is expected to shorten the software development time. Another merit of using CompactRIO is its maintainability when the FPGA used is updated, because LabVIEW is expected to absorb the difference between different FPGA versions.

Based on the above considerations, CompactRIO has greater merit for us. Therefore, we have been developing a prototype with a scale sufficient to conduct performance tests for the CompactRIO system, as shown in Fig. 2, since November 2021.

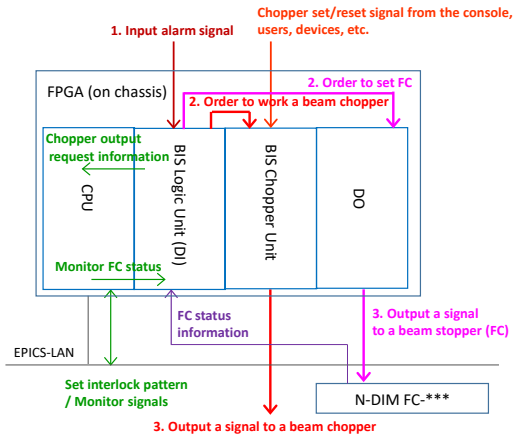

Fig. 2. Hardware constitution and process flow of the FPGA-BIS prototype using CompactRIO. FPGA is mounted on the chassis to which each module is installed.

References

1) M. Komiyama *et al.*, RIKEN Accel. Prog. Rep. **39**, 239 (2006).
2) M. Komiyama *et al.*, Proc. ICALEPCS2019, (2019), p. 384.
3) Yokogawa Electric Corporation, "Catalog of F3DF01-0N," unpublished.
4) CompactRIO, `https://www.ni.com/ja-jp/shop/compactrio.html`.
5) LabVIEW, `https://www.ni.com/ja-jp/shop/labview.html`.

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