

Accelerator report INTT onlmon progress summary 2023

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The sPHENIX OnlMon framework is designed to facilitate the monitoring of detector subsystems during data collection. Raw data is continuously unpacked and used to maintain ROOT¹⁾ histograms stored on a server. A client can request these histograms and use them to convey information to a user via a graphical interface, also generated using ROOT.¹⁾ Each subsystem of the sPHENIX experiment is responsible for implementing the unique methods needed for its framework.

The Intermediate Silicon Tracker (INTT) subsystem's implementation must be sufficiently comprehensive to show the readout status of the smallest partitions of its active area, yet compact enough so that a user can diagnose any issue at a glance. The hardware of the INTT is organized into four concentric layers of 12, 12, 16, 16 ladders (innermost layer to outermost layer). Each ladder is divided into north and south halves, and each half-ladder has 26 chips arranged in 2 rows of 13. Each chip has 128 channels which can further specify an analogue to digital conversion (ADC) value ranging 0 to 7. This is too much to show concurrently, and the compromise is to have multiple types of displays.

The GUI has two types of displays: a main display that shows the INTT at the level of individual chips, and a secondary display that will show an individual chip at the level of channels or ADC values. The main display exhibits four histograms, representing each layer, with a bin for each chip. The bin will be colored depending on a user specified option, such as the raw number of counts registered to the chip, a weighted-average ADC value, or the number of channels exhibiting statistically significant behavior when compared to others at similar pseudorapidity (Fig. 1).

From the main display, a user can click a bin to launch a second GUI that shows a single histogram representing the chip, with bins for each channel and possibly ADC value, again colored by the same user specified option, the raw number of counts in each channel,

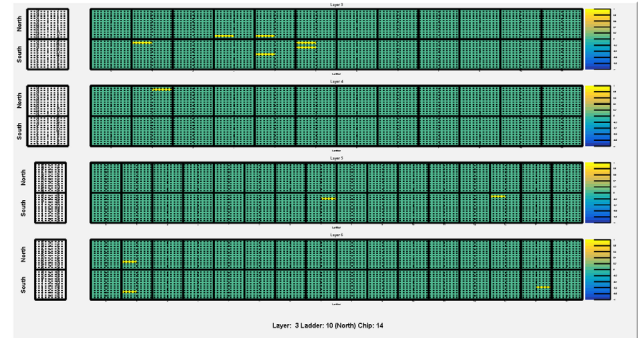


Fig. 1. A primary GUI where bin values are the number of statistically significant channels (see Fig. 2) in the chip the bin represents. In this case, there are only 12 chips with at least one significant channel (the yellow bins). Thick, black lines denote ladders and their north/south halves, thin dotted lines denote chips, a key shows the chip layout in one ladder, and text shows which chip the user's mouse is over.

the exact ADC distribution across all channels, or the likelihood of an issue with the channel based on its comparative performance (Fig. 2).

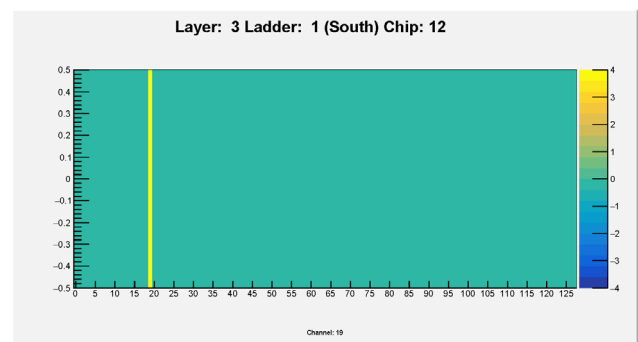


Fig. 2. A secondary GUI where bin values are the statistical significance (z -score) of the channel it represents when compared to all channels at similar pseudorapidity. Here, any $z < -2$ or $z > +2$ is considered significant and will be colored differently; in this case, there is only one (the yellow bin). Text at the bottom shows which channel the user's mouse is over.

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Reference

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